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EXAMINER	
MONDT, JOHANNES P	

ART UNIT	PAPER NUMBER
3663	

DATE MAILED: 11/27/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/750,843	RHODES, HOWARD E.	
	Examiner	Art Unit	
	Johannes P. Mondt	3663	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 September 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *19-27 and 66-80* is/are pending in the application.

4a) Of the above claim(s) *73-77* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *19-27,66-72 and 78-80* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 November 2005* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

Amendment filed 9/15/06 forms the basis for this office action. In said Amendment applicant substantially amended all claims drawn to the elected invention (19—27, 66-72 and added new claims 78-80. Claims 1-18 have previously been cancelled and claims 73-77 have previously been withdrawn.

Drawings

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "integration period" (see claims 19, 66 and 80) must be shown or the feature canceled from the claims. No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New

Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

1. The Specification is objected to because the "integration period" (see claim 19) has neither been defined nor disclosed. In particular, although the existence of an integration period is inherent to an imager in which accumulation of charge at a photo-conversion device takes place, its finish time is not disclosed in the specification. The absence of a shutter is not disclosed in the Specification. The Specification (patent documents incorporated by reference included) fails to specifically teach the absence of a shutter in the method as disclosed. Although with or without a shutter the integration period is defined for those of ordinary skill in the art as the period during which the photo-conversion device accumulates the charge some of which is transported to the charge collection region for read-out some question remains on whether or not accumulation of charge in the photo-conversion device 50 takes place during an interval within the period during which the RESET gate is activated because charge may flow faster in rather than out of the photo-conversion device during the ON state of the transfer gate. Furthermore, although the photoconversion device overall loses charge

carriers during the ON state of the transfer gate it also accumulates charges because of the pair production from incoming light. While the start of the integration period is taught to be the time transfer gate 26 is turned OFF the exact timing of the end of the "integration period" is not defined, and thereby the limitation "wherein the integration period and said reset period occur while a row select transistor in the first pixel cell is activated" is not disclosed.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. The Specification is objected to because the "integration period" (see claim 19) has neither been defined with regard to its termination time, nor with regard to a specific characteristic of the timing chart. In particular, although the existence of an integration period is inherent to an imager in which accumulation of charge at a photo-conversion device takes place, its finish time is not disclosed in the specification. The absence of a shutter is not disclosed in the Specification. The Specification (patent documents incorporated by reference included) fails to specifically teach the absence of a shutter in the method as disclosed. Although with or without a shutter the integration period is defined for those of ordinary skill in the art as the period during which the photo-conversion device accumulates the charge some of which is transported to the charge collection region for read-out some question remains on whether or not accumulation of charge in the photo-conversion device 50 takes place during an interval within the period during which the RESET gate is activated because charge may flow faster in

rather than out of the photo-conversion device during the ON state of the transfer gate. Furthermore, although the photo-conversion device overall loses charge carriers during the ON state of the transfer gate it also accumulates charges because of the pair production from incoming light. While the start of the integration period is taught to be the time transfer gate 26 is turned OFF the exact timing of the end of the "integration period" is not defined, and thereby the limitation "wherein the integration period and said reset period occur while a row select transistor in the first pixel cell is activated" is indefinite because the end point in time of said integration period is indefinite.

Claim Objections

3. ***Claim 22*** is objected to because of the following informalities: "said act of transferring" should be replaced by "said act of removing". Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

1. ***Claims 19-27, 66-72 and 78-80*** are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claims contain subject matter not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor, at the time the application was filed, had possession of the claimed invention.

In particular, although the existence of an integration period is inherent to an imager in which accumulation of charge at a photo-conversion device takes place, its finish time is not disclosed in the specification. The absence of a shutter is not disclosed in the Specification: in at least one embodiment considered equivalent to a photodiode, i.e., a photogate (see page 8-9, [0037]), a shutter is in fact included for each pixel. In addition, transistor 25 represents a global shutter (pages 8-9, [0037]). The Specification (patent documents incorporated by reference included) fails to specifically teach the absence of a shutter in the method as disclosed in any of the embodiments. Although with or without a shutter the integration period is defined for those of ordinary skill in the art as the period during which the photo-conversion device accumulates the charge some of which is transported to the charge collection region for read-out some question remains on whether or not accumulation of charge in the photo-conversion device 50 takes place during an interval within the period during which the RESET gate is activated because charge may flow faster in rather than out of the photo-conversion device during the ON state of the transfer gate. Furthermore, although the photo-conversion device overall loses charge carriers during the ON state of the transfer gate it also accumulates charges because of the pair production from incoming light. While the start of the integration period is taught to be the time transfer gate 26 is turned OFF the exact timing of the end of the "integration period" is not defined, and thereby the limitation "wherein the integration period and said reset period occur while a row select transistor in the first pixel cell is activated" is not disclosed.

2. ***Claims 66 and 80*** are additionally rejected under 35 USC 112, first paragraph, for the same reasons because of the explicit reciting of the undisclosed end point of the "integration period". See lines 2 in both claims.

   The following is a quotation of the second paragraph of 35 U.S.C. 112:

   > The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. ***Claims 19-27, 66-72 and 78-80*** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The reasons for this rejection are the same as the reasons for the objection to the Specification for indefiniteness (see section 2 under "Specification").

   In particular, by virtue of the undisclosed extent of the "integration period" (see above under objection to the Specification) the limitation "wherein said integration period and said reset period occur while a row select transistor in the first pixel cell is activated" is indefinite, the precise end point in time of said integration period not having been disclosed.

4. ***Claims 66 and 80*** are additionally rejected under 35 USC 112, first paragraph, for the same reasons because of the explicit reciting of the undisclosed end point of the "integration period". See lines 2 in both claims.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. ***Claims 19-25, 66-71 and 79*** are rejected under 35 U.S.C. 102(b) as being anticipated by Eguchi et al (US 2002/0051229 A1).

This rejection is offered subject to the noted indefiniteness under 35 USC 112, see above; assuming that the integration period may be defined by a period between a turning OFF of the transfer gate and the very first turning ON of said transfer gate following said turning OFF.

Eguchi et al teach (title, abstract, [0038]-[0061]) a method for operating a first pixel cell of an imager, the method comprising:

accumulating charge at a photo-conversion device (photodiode "a" also denoted by 1; see Figure 4 and Figure 6, and [0039]-[0042]) during an integration period (said integration period starts at the dotted line to the left and continues well into the ON state of the row select signal ϕ_{SEL} until the very first next ϕ_{TX} pulse ([0059]-[0061]);

resetting a charge collection region 11 (floating diffusion region; see [0040] and Figures 3, 6 and 10) with a reset transistor 3 ([0040]) during a reset period (said resetting is carried out by turning the reset transistor into the ON state (high ϕ_{RES}) as

delineated by Figure 7, said reset period being the period during which the reset transistor is ON (high) starting from the beginning of the time trace in Figure 7), wherein said integration period and said reset period occur while a row select transistor 6 ([0013] and [0040]) in said first pixel cell is activated (Figure 7 and [0059]-[0061]; note that the interval between the first ϕTX and second ϕTX pulse (=integration period, defined as the time interval between the first time the transfer gate is turned OFF until the first time after said first turning off that said transfer transistor is again switched ON: see [0048]) overlaps with a period during which the select transistor is activated (i.e., period of high ϕSEL));

storing accumulated charge from said photo-conversion device at said charge collection region via a transfer transistor 2 ([0039] and Figures 3 and 6);

reading out said charge from said charge collection region ([0050]); and

removing residual charge remaining in said photo-conversion device after said charge storage at said charge collection region (by activating simultaneously the reset transistor and the transfer transistor: see Figure 7); said act of removing comprises activating said reset transistor and said transfer transistor prior to a subsequent integration period (loc.cit.).

On claim 20: said act of removing comprises activating said reset transistor 3 and said transfer transistor 2 substantially simultaneously (as discussed under claim 19; see again Figure 7).

On claim 21: said substantially simultaneous activation of said reset transistor and said transfer transistor occurs after said act of reading out said charge (said act of

reading out said charge is realized by having high ϕ_{RESET} following an integration period terminated by the second pulse of ϕTX (Figure 7).

On claim 22: said act of transferring (interpreted as said act of removing, being accomplished by the transfer transistor followed by; see "Claim Objections" overleaf) comprising transferring charge from said photo-conversion device 1 to a supply voltage 4 ([0040]) (see objection to "Vdd" above under "Claim Objections": voltage V_{PR} supplies a voltage to reset 11 and hence can be called "supply voltage").

On claim 23: the imager by Eguchi et al is a CMOS imager ([0005]).

On claim 24: the CMOS imager comprises in one embodiment a four-transistor (Figure 3), in a second embodiment a five-transistor (Figure 6), and in a third embodiment, a six-transistor (Figure 8) pixel architecture.

On claim 25: the photo-conversion device is a photodiode 1 ([0039]).

*On claim 66:*N.B.: this rejection is offered subject to the noted indefiniteness of the integration period. Said reset period is immediate prior to said integration period to the extent integration period is understood as an interval defined by a starting time at which the transfer gate is turned OFF and a termination time at which the transfer transistor is switched ON again for the first time since the start time. The reset period is immediately prior (i.e., in the only manner disclosed in the specification based on the above assumption on integration period: namely, "is" as "exists": said reset period exists immediately prior to said integration period (Fig. 6c of the Specification), as witnessed by Figure 7, showing the reset transistor to be ON immediately prior to the first time the transfer transistor is turned OFF.

On claim 67: reading out said charge from said charge collection region comprises operating a transistor (source follower or amplifier transistor 10 ([0042] and [0050]) for reading out said charge as a pixel signal to a read-out circuit 13/15 (comprising vertical line 13 and transfer gates 15 ([0050]-[0051]).

On claim 68: the method further comprises storing said pixel signal in a sample and hold circuit 16 ([0051]).

On claim 69: activating said reset transistor 3 and said transfer transistor 2 substantially simultaneously comprises applying a reset signal to activate a gate of said reset transistor 3, and while said reset transistor is activated, applying a transfer signal ϕ_{TX} ([0045] and Figures 3, 6 and 8) to activate a gate of said transfer transistor 2 (see Figure 7: while ϕ_{RES} is high (reset transistor is ON).

*On claim 70:*said reset transistor is de-activated before said transfer transistor is de-activated (compare signal traces of ϕ_{RES} and ϕ_{TX} in Figure 7).

*On claim 71:*said transfer transistor is de-activated before said reset transistor is de-activated (compare the traces in timing chart Figure 7 of ϕ_{TX} and ϕ_{RES}).

On claim 79: the act of removing residual charge occurs while the row select transistor is not activated (Figure 7: ϕ_{SEL} is low (the row select transistor is OFF while.ϕ_{RES} and ϕ_{TX} are high (reset and transfer transistors ON)).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and

the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. ***Claims 26-27*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Eguchi et al as applied to claim 19, in view of Rhodes (6,500,692 B1).

As detailed, Eguchi et al anticipate claim 19.

Eguchi et al do not necessarily teach the further limitations defined by claims 26 or 27. *However, it would have been obvious* to include said further limitations in view of Rhodes, who, in a patent on CMOS imager technology, hence analogous art, teach said CMOS imager may be constituted with either a photodiode, a photo-gate or a photoconductor (col. 2, l. 6-20). There thus appear to be equivalent material embodiments for the operation of a CMOS imager. *Applicant does not disclose* in the Specification *why* the selection among photodiode, photo-gate and photoconductor is *critical* to the invention. In fact, the evidence of Applicant's position in this regard is in evidence because of claims 25-27, respectively claiming that said photo-conversion device is a photodiode (i.e., abutting oppositely conductive semiconductor layers), a photo-gate (laminate of gate and semiconductor material depletable by said gate) or a photoconductor (photoconductive material, which already is inherent in the former embodiments, because photon-induced electron-hole-pair production increases the electric conductivity). Applicant is reminded in this regard that it has been held that mere selection of known materials generally understood to be suitable to make a device, the selection of the particular material being on the basis of suitability for the intended use, would be entirely obvious. In re Leshin 125 USPQ 416.

7. ***Claims 72 and 78*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Eguchi et al as applied to claim 20 and 19, respectively.

Eguchi et al anticipate claims 20 and 19. Eguchi et al do not necessarily disclose the further limitation as defined by claim 72 or 78.

However, applicant in his disclosure does not explain why the further limitations are critical to the invention. On the contrary, with regard to claim 72, on pages 7-8, [0034] of the Specification, applicant explains that all that matters in this regard is that activation of reset and transfer transistors are carried out "substantially simultaneously", serving the purpose to sweep residual charge out of the photo-conversion device or photodiode 50, explaining furthermore, that "substantially simultaneously" applies to all figures 7 (a-d). There is no requirement regarding the relative turn-OFF and turn-ON times of reset and transfer transistor (see also [0031] on page 7 of the Specification). From this portion of the Specification and from the joint inclusion of claims 69 and 72 it is evidenced that there is no criticality as to the chronology of the turning ON of transfer and reset transistors, i.e., the value of the ratio of turn-ON times of transfer transistor over reset transistor may be =1, >1 or <1.

Similarly, with regard to claim 78, both mutually exclusive and jointly fully comprehensive alternatives are disclosed in the Specification with regard to whether the ROW select transistor is activated (Fig. 6a) or not activated (Figure 6b). In view of the absence of a teaching why a range is critical to the invention Applicant is reminded that it has been held that where the general conditions of a claim are disclosed in the prior

art, discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

8. ***Claim 80*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Eguchi et al as applied to claim 19, in view of Yadid-Pecht et al (IEEE Transactions on Electron Devices 44(10), pages 1721-1723; October 1997).

As detailed above, Eguchi et al anticipate claim 19. Eguchi et al do not necessarily teach the further limitation defined by claim 80. However, it would have been obvious to include said further limitation in view of Yadid-Pecht, who, in a publication on CMOS imager technology drawn to mitigate a/o large temporal noise (see page 1721, second paragraph, left column), hence analogous art, teach the integration period to vary among pixels (II. "Dual Sampling Approach", pages 1721-1722, especially page 1721, right column, formulae for T1int and T2int) so as to be able to view both the bright portions as well as the darker portions (first column of page 1722). *Motivation* to include the teaching by Yadid-Pecht et al derives immediately from the generic nature of the desirability to view all portions in an image well regardless variation in brightness among said portions (improved dynamic range; see, in addition to the cited portions, title, abstract and Introduction in Yadid-Pecht).

Response to Arguments

Applicant's arguments filed 9/15/06 have been fully considered but they are not persuasive because although an integration period as claimed in itself is inherent to an imager, the timing of said integration period, now by amendment critical to patentability, has not been disclosed in the original specification. In particular, the claimed subject

matter is mostly generic to processes that utilize shutters, such as a photo-gate or mechanical shutter, and those that do not have a need for it. A specific termination step or time has not been disclosed. Therefore, the integration period, in its timing and duration, has not been disclosed, and the claimed subject matter is both new matter and indefinite. See rejections under 35 USC 112, first and second paragraph, and objection for the same reason to the Specification and Drawings.

Furthermore, examiner regrets to have found pertinent art for all pending claims in the form of Eguchi et al; see the above rejections. For this reason the present action has been made non-final.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Johannes P. Mondt whose telephone number is 571-272-1919. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack W. Keith can be reached on 571-272-6878. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JPM
November 22, 2006

Patent Examiner:

Johannes Mondt (Art Unit: 3663)